REMARKS

The following remarks are made in response to the Office Action mailed October 19, 2005. Claims 1-24 were rejected. With this Response, no claims have been amended. Claims 1-24 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

Claims 1-5 and 12-16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regards as the invention. Regarding independent claims 1 and 12, the Examiner submits that the relationship between the stored previous privilege level and the first privilege level is unclear. The Examiner states that it is unclear as to what privilege level is being stored as a previous privilege level. (Office Action, page 3).

Claims 1 and 12 do not require a relationship between the previous privilege level state and the first privilege level. For example, in one embodiment the previous privilege level state is stored by a call instruction. (Specification at page 10, lines 3-5). The previous privilege level state could be any privilege level stored by the call instruction. Therefore, there is no need to provide a relationship between the stored previous privilege level state and the first privilege level.

In view of the above, independent claims 1 and 12 clearly define and distinctly claim the invention. Dependent claims 2-5 and 11-16 further define patentably distinct claims 1 and 12 respectively. Accordingly, Applicants respectfully submit that claims 2-5 and 11-16 are also allowable. Therefore, Applicants respectfully request that the rejections to claims 1-5 and 12-16 under 35 U.S.C. § 112 be withdrawn claims 1-5 and 12-16 be allowed.

Claim Rejections under 35 U.S.C. § 103

Claims 1-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the Arora U.S. Patent No. 6,393,556 in view of the Mattison U.S. Patent Application Publication No. 2002/0069316.

Applicants submit that the Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the invention of independent claims 1, 6, 12, 17, and 23.

The Arora Patent discloses changing a privilege level in a processor configured to pipeline instructions. The processor includes a first memory storing an architectural privilege level that is set at a first privilege level, a second memory storing a plurality of instructions, and a pipeline including a plurality of processing stages. A first instruction is fetched from the memory and a determination is made whether the first instruction requires the first privilege level be changed to a second privilege level, and in response thereto, any subsequent instructions are flushed from the pipeline before recording the second privilege level in the first memory. (Abstract).

In the Arora Patent, the processor 30 maintains a "current privilege level" (CPL) 38 in a memory storage device. The CPL is maintained in the processor's register set. The operating system sets the CPL to prevent the user from performing dangerous or insecure operations. If the pipeline 30 is currently processing an application program instruction, a prior instruction would have set the CPL 38 to the proper privilege level. If an instruction requiring a higher privilege level follows the current instruction, an instruction, such as an "enter privilege code" (EPC) instruction, that directs the processor to change the privilege level of the CPL must first be processed to increase the privilege level. (Col. 4, lines 13-27).

In the Arora Patent, after decoding an instruction directing the processor to change the CPL 38 from a first to a second privilege level, the processor compares the second privilege level to the CPL 38. (Col. 6, lines 27-31). The processor will compare the CPL 38 with the privilege level specified in the EPC instruction. If the EPC instruction directs the processor to change the CPL 38 to a higher privilege level, the processor flushes any instructions in the pipeline subsequent to the EPC instruction, and continues processing the EPC instruction. When the EPC instruction is retired, the CPL 38 privilege level is increased. If the EPC instruction specifies a privilege level lower than or the same as the CPL 38, the processor will issue a fault. (Col. 6, lines 46-59).

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest **performing a privilege promotion instruction by the operating system,**

the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level as recited in independent method claim 1.

The Examiner admits that the Arora Patent does not disclose storing the privilege level promotion instruction in a page of memory not writable by application instructions at a first privilege level. (Office Action, page 5). The Examiner submits that the Mattison Publication discloses this claim limitation in paragraphs 0015 and 0016.

The Mattison Publication discloses a method and apparatus for protecting flash memory such as a Basic Input/Output System (BIOS) from any unauthorized reprogramming efforts. The system includes a memory controller that provides a mode where the processor is restricted to accessing only the flash memory (i.e., a mode where the processor can only execute instructions from the flash memory and not from any other memory such as main system memory or cache). This mode can be enabled or disabled by setting or clearing a control register of the system memory controller. In addition, the memory controller incorporates a set of registers that can be used to define limited regions of accessibility to memory space outside flash memory. These registers are accessible to the processor only when the controller is operating in the restricted access mode. The register set consists of one or more pairs of registers, wherein each pair consists of a base register and a limit register. The base and limit registers define a memory region beyond the flash memory which would be accessible to the processor when the system is operating in the restricted mode. (Paragraphs 0015-0016).

The flash memory protection disclosed by the Mattison Publication does not teach or suggest the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level as recited in claim 1. The flash memory protection system disclosed by the Mattison Publication is not related to privilege levels. In contrast, the flash memory protection system is just a mode of operation initiated

by a flash memory upgrade program. (Paragraph 0019). The Mattison Publication fails to teach or suggest privilege levels or a first page of memory not writable by application instructions at a first privilege level.

The Examiner states that the claim 1 limitations of reading a stored previous privilege level state and comparing the read previous privilege level state to the current privilege level is disclosed in column 6, lines 46-49 of the Arora Patent. (Office Action, page 4). The Examiner also states that the previous privilege level state is disclosed by CPL 38 of the Arora Patent. (Office Action, page 4). In addition, the Examiner states that "comparing the current privilege level to the instructions privilege level wherein this case the instruction's privilege level is the current privilege level and the stored privilege level is the previous privilege level." (Office Action, page 4).

The cited text of the Arora Patent discloses comparing the architectural CPL with the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent fails to disclose the claim 1 limitations of *reading a stored previous privilege level state* and *comparing the read previous privilege level state to the current privilege level.* In the Arora Patent, a previous privilege level state is not stored and therefore cannot be read.

The Arora Patent also discloses that the CPL is compared to the privilege level specified in the EPC instruction. In contrast, claim 1 requires comparing the *read previous privilege level state* to the *current privilege level.* The privilege level of the EPC instruction does not teach or suggest the current privilege level. Rather, the EPC instruction directs the processor to change the privilege level of the CPL. (Col. 4, lines 24-26). The EPC instruction provides a future privilege level, not the current privilege level.

The Examiner states that the claim 1 limitations of "if a previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level" are disclosed by the Arora Patent "since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level . . .". (". . . increase the architectural current privilege level from privilege level 3 to privilege level 0"). (Office Action, page 4). The Examiner further states that, in comparing privilege levels, it is understood that the stored privilege level must be read in the comparison process. (Office Action, page 4).

The Arora Patent discloses raising the current architectural CPL to the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent, however, does not disclose the claim 1 limitation of promoting the current privilege level to a second privilege level which is higher than the first privilege level if the previous privilege level state is equal to or less privileged than the current privilege level.

Claim 1 recites if the *previous privilege level state* is equal to or *less privileged* than the *current privilege level*, promoting the current privilege level. In contrast, the Examiner states that the Arora Patent discloses increasing the *current privilege level* if the privilege level of the *CPL* is *lower* than the privilege level of the *EPC*. In addition, the Examiner states that the privilege level of the EPC instruction discloses the current privilege level state and the CPL discloses the stored previous privilege level state. (Office Action, page 2). Therefore, based on the Examiner's interpretation, claim 1 would recite if the CPL is equal to or less privileged than the privilege level of the EPC instruction, promoting the current privilege level. The CPL, however, is the current privilege level, not the previous privilege level state, and the privilege level of the EPC instruction is a future privilege level, not the current privilege level as submitted by the Examiner.

Further, there is no teaching or suggestion to combine the Arora Patent with the Mattison Publication in a manner that would provide the invention of independent claim 1. The Arora Patent is directed to an apparatus and method for changing a privilege level in a processor configured to pipeline instructions. In contrast, the Mattison Publication is directed to a method and apparatus for protecting flash memory and is not related to pipeline instructions or privilege levels. The Arora Patent and the Mattison Publication address unrelated problems. One skilled in the art would not look to the Mattison Publication when designing an apparatus and method for changing privilege levels. One skilled in the art could not combine the apparatus and method for changing the privilege level in a processor configured to pipeline instructions of the Arora Patent with the flash memory protection system of the Mattison Publication in a manner that would provide the invention recited by independent claim 1.

In view of the above, Applicants believe independent claim 1 to be allowable over the Arora Patent and the Mattison Publication. Dependent claims 2-5 further define patentably

distinct independent claim 1. Accordingly, dependent claims 2-5 are also believed to be allowable over the art of record.

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest **performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including: storing the first privilege level in a previous privilege level state; and performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including: reading the stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level** as recited in independent method claim 6.

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent and the Mattison Publication fail to teach or suggest the above limitations of claim 6, which are similar to the above limitations of claim 1.

In view of the above, Applicants believe independent claim 6 to be allowable over the cited references. Dependent claims 7-11 further define patentably distinct independent claim 6. Accordingly, dependent claims 7-11 are also believed to be allowable over the art of record.

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the computer system of independent claim 12 including **a memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the first memory page is not writeable by application instructions at a first privilege level;** and **performing the privilege promotion instruction as follows: reads the previous level state; compares the read previously privilege state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than a first privilege level.**

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the computer system of independent claim 17 including **a memory having a plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privileged routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level; wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows: stores the first privilege level in a previous privilege level state; and wherein the operating system performs the privilege promotion instruction as follows: reads the stored previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

The Arora Patent and the Mattison Publication, either alone, or in combination, fail to teach or suggest the computer readable medium of independent claim 23 containing a privilege promotion instruction for controlling a computer system to perform a method including **reading a stored previous privilege state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.**

For the same reasons as discussed above with reference to independent claim 1, the Arora Patent and the Mattison Publication fail to teach or suggest the above limitations of independent claims 12, 17, and 23, which are similar to the above limitations of independent claim 1.

In view of the above, Applicants believe independent claims 12, 17, and 23 to be allowable over the cited references. Dependent claims 13-16 further define patentably distinct independent claim 12. Dependent claims 18-22 further define patentably distinct independent claim 17. Dependent claim 24 further defines patentably distinct independent

claim 23. Accordingly, dependent claims 13-16, 18-22, and 24 are also believed to be allowable over the art of record.

In view of the above, Applicants respectfully request that the rejections to claims 1-24 under 35 U.S.C. § 103(a) be withdrawn and that claims 1-24 be allowed.

CONCLUSION

In view of the above, Applicants respectfully submit that pending claims 1-24 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to either David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854 or Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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